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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,866	03/22/2001	Kiichi Hirano	107318-00000	6213

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EXAMINER

GEBREMARIAM, SAMUEL A

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/813,866

Applicant(s)

HIRANO ET AL.

Examiner

Samuel A Gebremariam

Art Unit

2811

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on 01 August 2002.

2a) This action is FINAL.      2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 60-69 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 60-69 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

- 1) Certified copies of the priority documents have been received.
- 2) Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
- 3) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)  The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 and 7.

4) Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_.

5) Notice of Informal Patent Application (PTO-152)

6) Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 60, 61 and 63, are rejected under 35 U.S.C. 103(a) as being unpatentable Ohtani et al US patent No. 5,854,096 in view of Hashizume JP patent No. 40328651A.

Regarding claims 60 and 66, Ohtani teaches a method of fabricating a semiconductor device particularly a thin film transistor, comprising the steps of: forming an amorphous silicon film on an insulating substrate 11; heat treating the amorphous silicon film by laser annealing, therein forming a polycrystalline silicon film 104; forming an impurity regions 108/109 in said polycrystalline silicon film; rapidly heat treating the impurity region by rapid thermal annealing (RTA) using laser beam and laser lamp as a heat source for rapidly heat-treating the impurity region to activate the impurity region (figs. 3a to 3e, column 13, lines 49-59 and columns 19, lines 16-39).

Ohtani fails to teach using a light source emitting sheet-type annealing light in order to activate the impurity region and crystallizing the amorphous silicon.

Hashizume teaches (abstract) using sheet shape beam for the purpose of annealing silicon layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the sheet-type laser beam taught by Hashizume in the process of Ohtani in order to obtain a uniform annealing in a certain direction.

Regarding claims 61 and 67, Ohtani teaches (col. 12, lines 58-68) substantially the entire claimed process step of claim 60 above including forming an insulating film of 2000 Å on the substrate and forming the amorphous silicon film on the insulating film.

Furthermore parameters such as thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired film quality during device fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the thickness of insulating film within the range as claimed in order to form the TFT.

Regarding claim 63 and 69, Ohtani teaches substantially the entire claimed process step of claims 60 and 66 above except explicitly stating that the rapid heat treating step comprise a step of preparing the light source by arranging a pair of lamps vertically opposed to each other and carrying the substrate so as to pass between the pair lamps.

It is conventional to position heat sources facing each other on opposite sides of the structure need to be heat treated. It would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the annealing environment by placing heat sources as claimed in order to get uniform annealing.

Claims 62 and 68, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani in view of Hashizume and in further view of Tajima JP patent No. 02194626.

Regarding claims 62 and 68, Ohtani teaches substantially the entire claimed process step of claim 60 above except explicitly stating that xenon arc lamp is used as heat source.

It is conventional and also taught by Tajima (abstract) to use xenon arc lamp as a light source to heat semiconductor structures.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the xenon arc lamp taught by Tajima in the process of Ohtani for annealing purposes.

Claims 64 and 65, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani in view of Hashizume and in further view of Rohatgi et al US patent No. 5,766,964.

Regarding claims 64 and 65, Ohtani teaches substantially the entire claimed process step of claim 60 above except explicitly stating that the process step of rapid thermal annealing is performed a plurality of times while the heating temperature is increased stepwise from an initial time to a final time.

Rohatgi teaches (column 8, lines 25-45) conducting RTA processing by initially ramping the temperature to a certain value and slowly increasing the temperature at rate of 43° C per second.

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching from Rohatgi in to the process steps of Ohtani since slowly ramping the temperature helps for a slow diffusion of impurities in to the silicon.

### ***Conclusion***

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B, C and O are cited as being related to thin film transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam  
October 17, 2002

*Tom* *Thomas*  
TOM THOMAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800